SUB B1

a clock signal connection to receive a clock signal;

an interconnect configuration that is compatible with a rambus dynamic random access memory (RDRAM);

A'cont

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal;

input circuitry to receive input data on the data connections at a rate of two data words per clock cycle; and

sense amplifier circuitry coupled to the array, wherein the sense amplifier circuitry detects a differential voltage.

19. (New) The flash memory of claim 18, wherein the memory is adapted to provide burst-oriented read accesses.